UNITED STATES PATENT AND TRADEMARK OFFICE

H·A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,062	07/31/2003	Bradley Ryan Harrington	AUS920030467US1	3513

35525 7590 08/15/2006

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER
PANTOLIANO JR, RICHARD

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,062	HARRINGTON ET AL.	
	Examiner	Art Unit	
	Richard Pantoliano Jr	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial office action for Application# **10/631,062** filed on **31 July 2003**.

Claims 1-24 are currently pending and have been considered below.

Specification

2. The disclosure is objected to because of the following informalities:

a) Page 8: The acronyms ISA, NVRAM and JTAG were not defined by Applicant; and

b) Page 12, last paragraph: The "hardware console" from Figure 2 is identified in the specification as element 264. However, Figure 2 does not contain an element marked 264, and the hardware console is clearly marked in the figure as element 280.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 4,12, and 20** rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention. The location at which the context of the stopped processor was not described within the specification. Examiner believes this to mean that any storage media, such as a hard disk drive or Random-Access Memory (RAM), are appropriate for storing the context of a processor.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 17 and 23 rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter. On page 19 of the specification, Applicant states that computer readable media include "transmission-type media, such as digital and analog communications links using transmission forms, such as...radio frequency and light transmissions." However, transmission-type media are, by definition, only capable of transmitting data. Since transmission-type media are incapable of retaining transmitted information, claims made to such media constitute non-statutory subject matter.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1, 6, 9, 14, 17, and 22** rejected under 35 U.S.C. 102(b) as being anticipated by Intel *("Itanium™ Processor Floating-point Software Assistance and Floating-point Exception Handling." January 2000)*.

Claims 1, 9, and 17: Intel discloses the method, system and computer readable medium for handling exception vectors by firmware comprising:

a) means and instructions for identifying an exception *(Page 2-2, ¶4-7)(The emulation library, a software means of accessing the firmware, recognizes the exception and handles it accordingly)*;

b) means and instructions for saving the identified exception *(Page 1-2, ¶4-6)*;

c) means and instructions replacing the exception vector with a substitute exception *(Page 2-2, ¶5 and ¶6)(The emulation library can call the kernel exception handler or a user level floating-point exception handler to continue processing the exception)*; and

d) means and instructions for restoring the saved exception when control is returned to the operating system *(Page 2-2, ¶4-7)(Control is returned to the operating system kernel exception handler before execution of the running program is resumed)*.

Claims 6, 14 and 22: Intel discloses the method, system and computer readable medium of **Claims 1,9, and 17**, respectively, for handling exception vectors by firmware

wherein the data processing system is a symmetric multiprocessor system *(Page 7-2, ¶4)*.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 2, 4, 5, 7, 8, 10, 12, 13, 15, 16, 18, 20, 21, 23 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel *("Itanium™ Processor Floating-point Software Assistance and Floating-point Exception Handling." Intel Corp., January 2000)* in view of Jones *(Jones, Steve. "Using spinlocks in a symmetric multiprocessing environment." Tech Specialist, v2, n10, pg 15(6), Oct 1991)*.

Claims 2, 10, and 18: Intel discloses the method, system and computer readable medium of **Claims 1,9, and 17**, respectively, for handling exception vectors, but does not disclose the use of a slave loop to suspend the operation of other processors in the system that attempt to access the same portion of firmware until the first process using that code has completed. Jones discloses the use of a spinlock (a slave loop) to pause the execution of a BIOS routine (a form of firmware) by processes other than the one currently processing the BIOS routine *(Jones, Pg 2, last paragraph and Pg 3, 3rd paragraph)*. It would have been obvious for one of ordinary skill in the art to combine

the teachings of Jones in using spinlocks to pause the execution of other processors in a Symmetric Multiprocessor system while accessing firmware into the system, method and computer readable medium of Intel in order to prevent disruption of computations caused by accessing code that should only be accessed by one program at a time *(Jones, Pg 1, last paragraph)*.

Claims 4, 5, 12, 13, 20 and 21: Intel and Jones discloses the method, system and computer readable medium of **Claims 2, 10, and 18**, respectively, but Intel does not disclose the storing of the processor context of the process placed in the slave loop or the restoring of said stored state when the processor is able to continue processing. Jones discloses the use of a spinlock (a slave loop) to pause the execution of a BIOS routine (a form of firmware) by processes other than the one currently processing the BIOS routine *(Jones, Pg 2, last paragraph and Pg 3, 3rd paragraph)*. It would have been obvious for one of ordinary skill in the art to combine the teachings of Jones in using spinlocks to pause the execution of other processors in a Symmetric Multiprocessor system while accessing firmware into the system, method and computer readable medium of Intel in order to prevent disruption of computations caused by accessing code that should only be accessed by one program at a time *(Jones, Pg 1, last paragraph)*. The use of a spinlock to pause the execution of a processor inherently requires that the state of the processor be saved because, while the processor keeps checking the state of the lock, it must use registers (memory locations local to the processor that are used to perform operations) previously occupied by the previous task being executed. The contents of the registers that corresponded to the information

relating to the exception must be stored in RAM or some other storage medium to allow the processor to continue with that exception, once the lock is held by that processor. Once that lock is held, the processor must inherently load that saved context back into the registers in order to continue its previous operation.

Claims 7, 8, 15, 16, 23 and 24: Intel discloses the method, system and computer readable medium for handling exception vectors comprising:

a) means and instructions for receiving control from an operating system *(Page 1-2, ¶4-6 and Page 2-2, ¶4-7)(The state of the interrupted process is saved, and the operating system exception handler passes calls the emulation library to handle the exception)*;

b) means and instructions for replacing an exception vector with substitute code (*Page 2-2, ¶4-7)(The state of the interrupted process is saved, and the operating system exception handler passes calls the emulation library to handle the exception)*; and

c) means and instructions for restoring the exception vector when control is returned to the operating system (*Page 2-2, ¶4-7)(Control is returned to the operating system kernel exception handler before execution of the running program is resumed).*

Intel does not disclose means and instructions for suspending execution of any other processor that tries to execute the same code with the use of a slave loop. Jones discloses the use of a spinlock (a slave loop) to pause the execution of a BIOS routine

(a form of firmware) by processes other than the one currently processing the BIOS routine *(Jones, Pg 2, last paragraph and Pg 3, 3rd paragraph)*. It would have been obvious for one of ordinary skill in the art to combine the teachings of Jones in using spinlocks to pause the execution of other processors in a Symmetric Multiprocessor system while accessing firmware into the system, method and computer readable medium of Intel in order to prevent disruption of computations caused by accessing code that should only be accessed by one program at a time *(Jones, Pg 1, last paragraph)*.

10. **Claims 3, 11, and 19 are** rejected under 35 U.S.C. 103(a) as being unpatentable over Intel *("Itanium™ Processor Floating-point Software Assistance and Floating-point Exception Handling." January 2000)* in view of Jones *(Jones, Steve. "Using spinlocks in a symmetric multiprocessing environment." Tech Specialist, v2, n10, pg 15(6), Oct 1991)* and in further view of IBM *(IBM Technical Bulletin: NNRD447149. "Method to Prevent Multiple Processes After Taking Exceptions To Enter Open Firmware In a Symmetrical Multiprocessor machine", Published 01 July 2001)*.

Claims 3, 11, and 19: Intel and Jones discloses the method, system and computer readable medium of **Claims 2, 10, and 18**, respectively, but does not disclose the use of processor identification numbers to identify the processor currently making exclusive use of the firmware and the processors trying to access that same portion of firmware that is already in use. IBM discloses the use of processor IDs in marking the lock used to identify which processor currently holds the lock on the firmware *(IBM, pg*

1, lines 23-27). It would have been obvious to one of ordinary skill in the art to combine the teachings of IBM into the method, system and computer readable medium of Intel and Jones to ensure that all processors in the system are aware of the fact that the lock is held by a processor and, in particular, which of the other processors in the system is the one that holds that lock.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a) Eilert et al. (US Pat: 4,809,157) discloses a system for managing hardware exception vectors in an SMP system;

b) Rothman et al. (USPG Pub: 2004/0123086) discloses a system for allowing software interrupts to access routines normally made available by the boot firmware of the computer; and

c) Lee (US Pat: 5,867,658) discloses a method for implementing a stop state for a processor in an SMP computer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Pantoliano Jr whose telephone number is (571) 270-1049. The examiner can normally be reached on Monday-Thursday, 8am - 4 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James W. Myhre can be reached on (571)270-1065. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RP
8/04/2006

James W. Myhre
Supervisory Patent Examiner